AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A digital delaying device for delaying an input signal with digital type, the digital delaying device comprising:

a ring oscillator having a plurality of delay cells connected in a loop, for outputting an oscillation clock;

a calibration unit for receiving a reference clock and the oscillation clock and calculating a pulse number of the oscillation clock corresponding to each reference clock period, the pulse number serving as a period reference pulse number;

at least one delay number calculation unit for receiving the period reference pulse number and a signal delay value, calculating a signal delay number corresponding to the signal delay value according to the period reference pulse number, and outputting a selection signal; ~~and~~

a set of flip-flop for synchronously outputting the selection signal and an input signal; and

at least one delay channel comprising a plurality of cascaded delay cells, the cascaded delay cells receiving ~~an~~ the input signal output from the set of flip-flop, generating a plurality of delay signals with different delay timings, and selecting and outputting one of the delay signals as an output signal according to the selection signal output from the set of flip-flop.

2. (Original) The digital delaying device according to claim 1, wherein the frequency of the oscillation clock is higher than that of the reference clock.

3. (Cancelled)

4. (Original) The digital delaying device according to claim 1, wherein the loop of the ring oscillator further comprises an NAND gate for receiving a reset signal to reset the ring oscillator.

5. (Currently Amended) ~~The digital delaying device according to claim 1,~~ A digital delaying device for delaying an input signal with digital type, the digital delaying device comprising:

a ring oscillator having a plurality of delay cells connected in a loop, for outputting an oscillation clock;

a calibration unit for receiving a reference clock and the oscillation clock and calculating a pulse number of the oscillation clock corresponding to each reference clock period, the pulse number serving as a period reference pulse number;

at least one delay number calculation unit for receiving the period reference pulse number and a signal delay value, calculating a signal delay number corresponding to the signal delay value according to the period reference pulse number, and outputting a selection signal; and

at least one delay channel comprising a plurality of cascaded delay cells, the cascaded delay cells receiving an input signal, generating a plurality of delay signals with different delay timings, and selecting and outputting one of the delay signals as an output signal according to the selection signal;

wherein the loop of the ring oscillator further comprises an NOR gate for receiving a reset signal to reset the ring oscillator.

6. (Currently Amended) ~~The digital delaying device according to claim 1, wherein the delay number calculation unit has~~ A digital delaying device for delaying an input signal with digital type, the digital delaying device comprising:

a ring oscillator having a plurality of delay cells connected in a loop, for outputting an oscillation clock;

a calibration unit for receiving a reference clock and the oscillation clock and calculating a pulse number of the oscillation clock corresponding to each reference clock period, the pulse number serving as a period reference pulse number;

at least one delay number calculation unit for receiving the period reference pulse number and a signal delay value, calculating a signal delay number corresponding to the signal delay value according to the period reference pulse number, outputting a selection signal, and having a calculation function of $F(m,M,C) = (m/M) * C$; and

at least one delay channel comprising a plurality of cascaded delay cells, the cascaded delay cells receiving an input signal, generating a plurality of delay signals with different delay timings, and selecting and outputting one of the delay signals as an output signal according to the selection signal;

wherein F(m,M,C) represents the signal delay number, M represents the number of minimum delay units contained in each reference clock period, m represents the signal delay value, and C represents the period reference pulse number.

7. (Original) The digital delaying device according to claim 1, wherein the calibration unit comprises:

a pulse generator for receiving the reference clock and generating a trigger signal at a rising edge of the reference clock;

a counter for receiving the trigger signal and the oscillation clock, and counting the pulse number of the oscillation clock, the trigger signal serving as a clear signal; and

a register for storing a count value of the counter, which serves as the period reference pulse number, according to the trigger signal.

8. ~~The digital delaying device according to claim 7, wherein the calibration unit further comprises~~ A digital delaying device for delaying an input signal with digital type, the digital delaying device comprising:

a ring oscillator having a plurality of delay cells connected in a loop, for outputting an oscillation clock;

a calibration unit for receiving a reference clock and the oscillation clock and calculating a pulse number of the oscillation clock corresponding to each reference clock period, the pulse number serving as a period reference pulse number, the calibration unit comprising:

a pulse generator for receiving the reference clock and generating a trigger signal at a rising edge of the reference clock;

a counter for receiving the trigger signal and the oscillation clock, and counting the pulse number of the oscillation clock, the trigger signal serving as a clear signal;

a register for storing a count value of the counter, which serves as the period reference pulse number, according to the trigger signal; and

a first frequency divider for dividing the frequency of the reference clock and inputting a frequency-divided reference clock to the pulse generator;

at least one delay number calculation unit for receiving the period reference pulse number and a signal delay value, calculating a signal delay number corresponding to the signal delay value according to the period reference pulse number, and outputting a selection signal; and

at least one delay channel comprising a plurality of cascaded delay cells, the cascaded delay cells receiving an input signal, generating a plurality of delay signals with different delay timings, and selecting and outputting one of the delay signals as an output signal according to the selection signal.

9. (Original) The digital delaying device according to claim 8, wherein the calibration unit further comprises a second frequency divider for dividing the frequency of the oscillation clock and inputting a frequency-divided oscillation clock to the counter.

10. (Original) The digital delaying device according to claim 9, wherein a frequency-divided value for the first frequency divider is the same as a frequency-divided value for the second frequency divider.

11. (Original) The digital delaying device according to claim 10, wherein the delay number calculation unit has a calculation function of:

$F(m,M,C)= (m/M) * C,$

wherein F(m,M,C) represents the signal delay number, M represents the number of minimum delay units contained in each reference clock period, m represents the signal delay value, and C represents the period reference pulse number.

12. (Original) The digital delaying device according to claim 9, wherein a frequency-divided value for the first frequency divider is different from a frequency-divided value for the second frequency divider.

13. (Original) The digital delaying device according to claim 12, wherein the delay number calculation unit has a calculation function of:

$F(m,M,C,A) = (m/M) * C * A,$

wherein F(m,M,C,A) represents the signal delay number, M represents the number of minimum delay units contained in each reference clock period, m represents the signal delay value, C represents the period reference pulse number, and A represents a multiple obtained by

dividing the frequency-divided value of the second frequency divider by the frequency-divided value of the first frequency divider.

14. (Original) The digital delaying device according to claim 1, wherein the delay cells of the ring oscillator and the delay cells of the delay channel have the same delay timing.